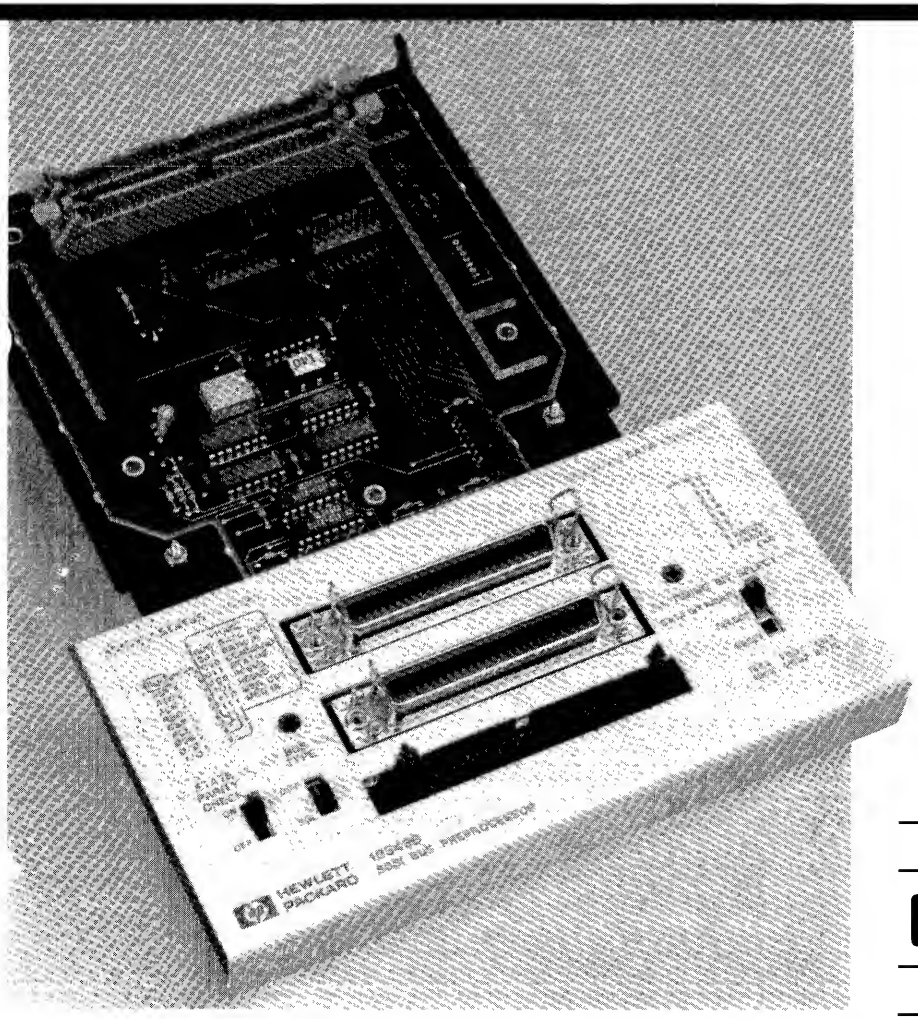
HP 10343B SCSI Bus Preprocessor
(HP 1630A/D/G and HP 1631A/D)

Operating Manual



HEWLETT PACKARD

Bus Preprocessor Operating Manual

HP 10343B
SCSI Bus Preprocessor

for the HP 1630A/D/G and HP 1631A/D Logic Analyzers

Manual Set Part Number 10343-90901
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Introduction

The HP 10343B Small Computer Systems Interface (SCSI) Bus Preprocessor provides a complete mechanical and electrical connection between your 8-Bit Single-Ended or Differential SCSI Bus system and the HP 1630A/D/G or HP 1631A/D Logic Analyzer.

The HP 10343B software provides inverse assembly of activity on the buses, and configurations for the logic analyzers. Any information about the usage of the HP 1630A/D/G or HP 1631A/D Logic Analyzers is supplementary to that provided in the logic analyzer operation and programming manuals.

This manual is organized into three chapters and two appendices.

Chapter 1 covers general information such as product description and accessories.

Chapter 2 covers the use of the HP 10343B for inverse assembly of your SCSI Bus system. This chapter includes installation procedures and other information specific to using the HP 10343B on the SCSI bus.

Chapter 3 contains general information about the software supplied, including information about inverse assembler operation.

Appendix A contains product specifications, general hardware information, and theory of operation.

Appendix B contains an overview of the Small Computer Systems Interface (SCSI). Additional information should be obtained from the appropriate standards organization for the SCSI Standard X3T9.2/86-109 Revision 2.

General Information 1

Introduction

The HP 10343B Small Computer Systems Interface (SCSI) Bus Preprocessor provides a complete mechanical and electrical connection between your 8-Bit Single-Ended or Differential SCSI Bus system and the HP 1630A/D/G or HP 1631A/D Logic Analyzer. With this equipment you can:

- Capture and analyze command sets and data activity for each of the SCSI device types specified in the SCSI Standard X3T9.2/86-109 Revision 2.
- Do Timing Analysis on SCSI Bus lines.
- Perform parity checking.
- Determine at a glance data and status conditions with the LED indicators on the HP 10343B.

The HP 10343B includes software to configure the logic analyzer for SCSI Bus analysis and inverse assemblers for 10 different SCSI device types. The inverse assemblers are all compatable to the HP 1630A/D/G and HP 1631A/D Logic Analyzers.

Power Requirements

The HP 10343B draws approximately 0.80 amps at +5 V from the HP 1630A/D/G or HP 1631A/D Logic Analyzer.

Input Loading

The even numbered signal lines have an input impedance of 5k ohms tied to 2.5 volts. The odd numbered signal lines have an input impedance of 10k ohms tied to 2.5 volts.

Each signal line has a maximum length of 10 centimeters inside of the interface to conform to the single-ended SCSI specification.

Outputs

The HP 10343B does not output any signals to the SCSI Bus.

Initial Inspection

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been inspected mechanically and electrically. If the contents are incomplete, if there is mechanical damage or a defect, or if the instrument does not operate, notify your nearest Hewlett-Packard Sales and Service Office. If the shipping container is damaged, or the cushioning materials show signs of stress, notify the carrier as well as Hewlett-Packard. Keep the shipping materials for inspection by the carrier.

Equipment Supplied

The equipment supplied with the HP 10343B consists of the following:

- One HP 10343B Preprocessor Module;
- One Shielded Cable (HP part number 8120-4998);
- Inverse assembly software on a 3.5-inch disc; and
- This operating manual.

Minimum Equipment Required

The following list is the minimum equipment required for a system using the HP 10343B SCSI Bus Preprocessor.

- HP 1630A/D/G or HP 1631A/D Logic Analyzer;
- HP 10269A/B General Purpose Probe Interface;
- HP 10343B SCSI Bus Preprocessor;
- HP 9121D/S or HP 9122D/S 3.5-inch flexible disc drive;
- One HP-IB cable; and
- One BNC cable.

SCSI Bus Preprocessing 2

Introduction

This chapter explains how to connect the HP 10343B SCSI Bus Preprocessor between your 8-Bit Single-Ended or Differential SCSI Bus system and the HP 1630A/D/G or HP 1631A/D Logic Analyzer. This includes loading the inverse assembler and configuring the logic analyzer.

Preprocessor Function

The HP 10343B SCSI Bus Preprocessor consists of an interface module which plugs into the HP 10269A/B General Purpose Probe Interface. The connectors on the HP 10343B accept both shielded and nonshielded SCSI bus cables which allow it to be connected quickly and easily into your SCSI Bus system. Switches on the front panel allow you to the select the appropriate bus type, parity, and SCSI lines to look at with timing. LED lights as indicators allow you to look at the static condition of the bus at a quick glance. The interface may be used with the HP 1630A/D/G and HP 1631A/D Logic Analyzers.

There are ten inverse assemblers available that can be loaded into the logic analyzer. This gives you the flexiblity of selecting the appropriate inverse assembler to decode any of the ten different device types that are called out in the SCSI Standard X3T9.2/86-109 Revision 2. These inverse assemblers are all compatable to the HP 1630A/D/G and HP 1631A/D Logic Analyzers.

Equipment Required

The minimum equipment required for a SCSI bus system using the HP 10343B SCSI Bus Preprocessor consists of the following:

- HP 1630A/D/G or HP 1631A/D Logic Analyzer;
- HP 10269A/B General Purpose Probe Interface;
- HP 10343B Bus Preprocessor;
- HP 9121D/S or HP 9122D/S 3.5-inch flexible disc drive;
- One HP-IB cable;
- One BNC cable; and
- This operating manual.

Installation Overview

1. Install the HP 10343B SCSI Bus Preprocessor in the HP 10269A/B General Purpose Probe Interface (see page 2-5).

2. Select the appropriate bus mode (Single-Ended or Differential) on the front panel of the HP 10343B (see page 2-7).

3. Select the parity setting on the HP 10343B that matches your system (see page 2-7).

4. Connect a BNC cable from the ACCESSORY POWER output on the rear panel of the logic analyzer to the ACCESSORY POWER input on the HP 10269A/B.

5. When using the HP 1630D or HP 1631D, connect the logic analyzer as follows:

Function	HP 1630D and HP 1631D Pod	(into)	HP 10269A/B Connector
State Data	2		A
State Status	3		B
Timing Data	0		C
Timing Status	1		D

When using the HP 1630A/G or HP 1631A, connect the logic analyzer as follows:

Function	HP 1630A/G and HP 1631A Pod	(into)	HP 10269A/B Connector
State Data	2		A
State Status	3		B
Timing Data	1*		C
Timing Status	1*		D

*Since only one pod (eight channels) are available for timing analysis on the HP 1630A/G and HP 1631A Logic Analyzers, only one group of timing lines (Data or Status) can be analyzed at one time.

6. Connect the HP 10343B SCSI Bus Proprecessor to your SCSI Bus system (see page 2-11).

7. Load the appropriate inverse assembler from the flexible disc (see page 2-16).

8. Load the configuration file into the logic analyzer by loading the file:

- "CSCSICON" for the HP 1630A/D and HP 1631A/D (see page 2-19);
- "CSCSICONG" for the HP 1630G (see page 2-19).

Note

You must reload the configuration file each time you load a different inverse assembler.

Installing the HP 10343B on the HP 10269A/B

To install the HP 10343B in the HP 10269A/B:

1. Install the HP 10343B on the bottom of the HP 10269A/B (see figure 2-1).

2. Install the metal tabs on the end of the HP 10343B in the slots of the HP 10269A/B.

3. Connect the two 60-pin cables from the HP 10269A/B to the connectors on the HP 10343B.

4. Fold the HP 10343B into the bottom of the HP 10269A/B and fasten the HP 10343B to the HP 10269A/B with the two captive screws.

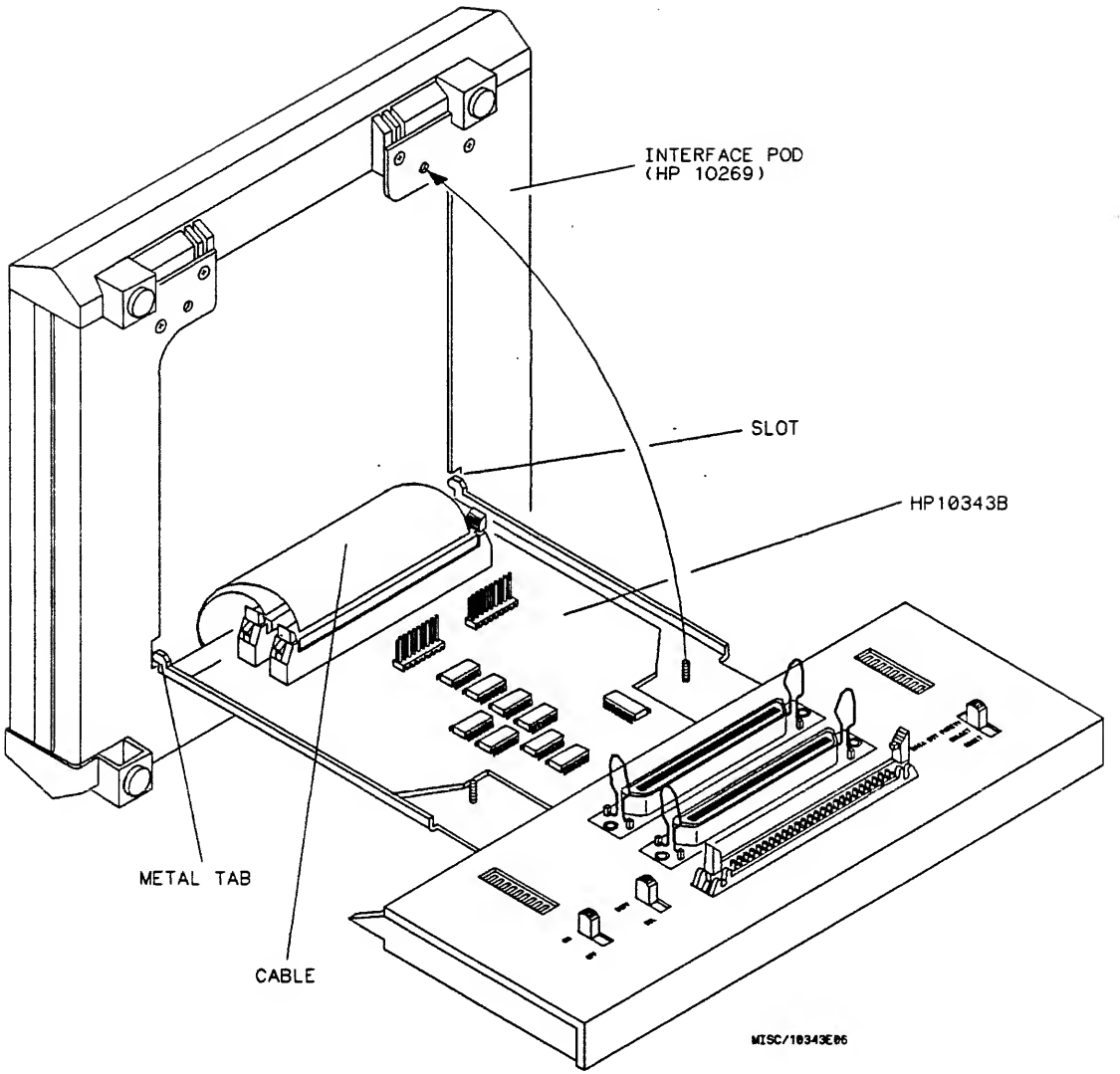


Figure 2-1. Installing the HP 10343B on the HP 10269A/B

Setting Up the HP 10343B Front Panel

The HP 10343B has three switches on the front panel (see figure 2-2):

Bus Mode. Allows the user to test either a Single-Ended or Differential Bus system. This switch setting must match the type of SCSI bus you are currently monitoring.

State Parity Check. The use of the parity bit is not manditory on a SCSI bus system. This switch allows the user to switch off the parity check.

Note

Excessive parity errors may appear on screen if parity is on with a system that does not use parity.

Timing Bit Select. This switch allows you to select the Parity, Select, or Reset lines for timing. The output of this selection is on Status bit 3 of pod 1 which connects to bucket D of the HP 10269A/B.

Note

HP 1630A/G and HP 1631A Logic Analyzers do not have enough timing channels to look at both the Timing Status and Data lines at the same time. To look at the Status or Data lines, you must manually move pod 1 of the logic analyzer between connector C (Data) and connector D (Status) of the HP 10269A/B. Only one group of timing lines can be seen at one time.

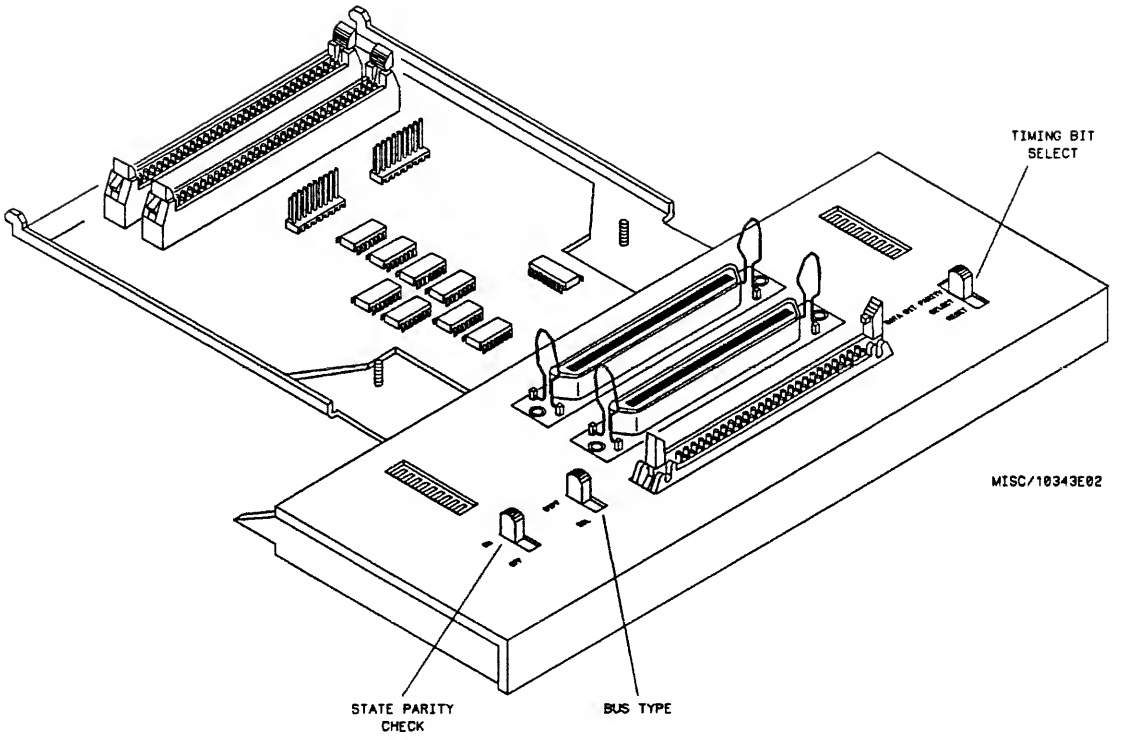


Figure 2-2. Switch Locations

Connecting to the HP 10269A/B

Connect a BNC cable from the ACCESSORY POWER output on the rear panel of the logic analyzer to the ACCESSORY POWER input on the HP 10269A/B.

Note

Some interface modules can draw up to 1 amp from the 5 volt supply of the logic analyzer. If you are using a coaxial cable, Hewlett-Packard recommends RG-58, 4 feet or less to minimize voltage drop.

When using the HP 1630D or HP 1631D, connect the logic analyzer as follows:

Function	HP 1630D and HP 1631D Pod	(into)	HP 10269A/B Connector
State Data	2		A
State Status	3		B
Timing Data	0		C
Timing Status	1		D

To use the HP 10343B with the HP 1630A/G or HP 1631A, connect up the probes as follows:

Function	HP 1630A/G and HP 1631A Pod	(into)	HP 10269A/B Connector
State Data	2		A
State Status	3		B
Timing Data	1*		C
Timing Status	1*		D

*Since only one pod (eight channels) are available for timing analysis on the HP 1630A/G and HP 1631A Logic Analyzers, only one group of timing lines (Data or Status) can be analyzed at one time.

Connecting the HP 10343B to the Bus

There are two types of connectors on the front panel (see figure 2-4).

- Two 50 Pin D-Shell shielded type; and
- One 50 Pin (dual rows of 25 Pins) connector of .100 inch spacing (nonshielded).

Shielded Cables

The user daisy chains the shielded connectors so both of them are used together. This is accomplished by the following steps:

1. Turn off the power to your bus system and logic analyzer.

2. Disconnect one end of a cable from your bus system and connect it to one of the shielded connectors on the HP 10343B.

3. Connect the shielded cable supplied with the HP 10343B from the other shielded connector on the HP 10343B to your bus system.

4. Turn on the bus and logic analyzer.

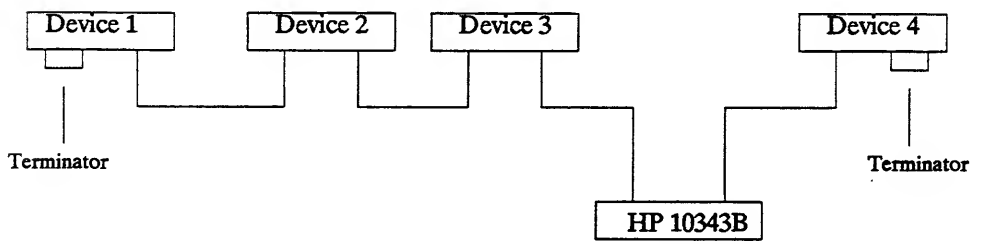


Figure 2-3. Connecting to the SCSI Bus

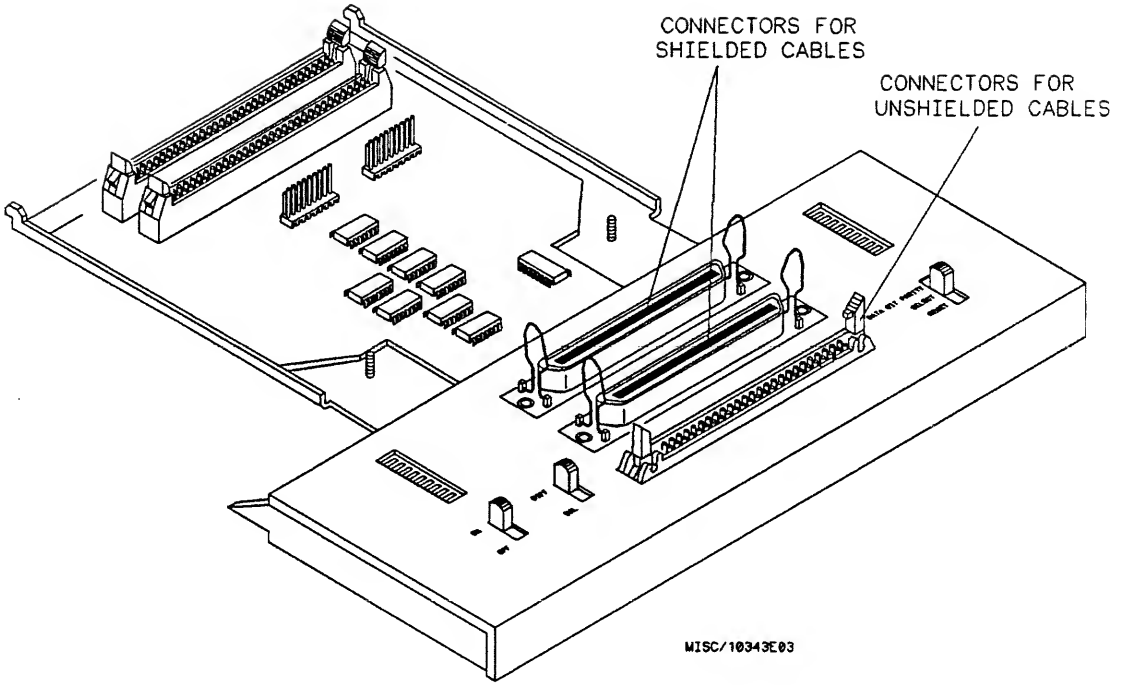


Figure 2-4. HP 10343B Bus Connectors

The HP 10343B can also be connected to one end of the bus by the following steps:

1. Turn off the power to your bus system and logic analyzer.

2. Remove a terminator from one end of your bus system.

3. Connect the shielded cable supplied with the HP 10343B from the shielded connector on the HP 10343B to the location on your bus system in which the terminator was located.

4. Connect the terminator to the unused shielded connector on the HP 10343B.

5. Turn on the bus and logic analyzer.

Note

The SCSI Bus system must be terminated at both ends for proper preprocessor operation.

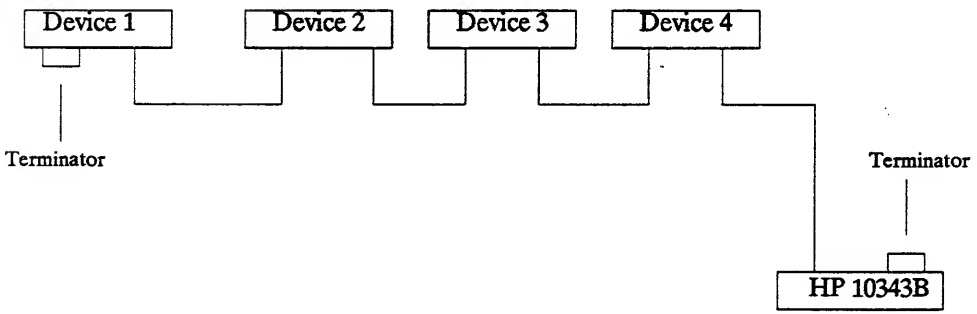


Figure 2-5. Connecting to the Bus

Nonshielded Cable

If a nonshielded SCSI ribbon cable is used with connectors clamped in the center of its length, it should be connected as follows:

1. Turn off the power to your bus system and logic analyzer.

2. Plug one of the connectors from the ribbon cable into the dual-row nonshielded connector on the HP 10343B.

3. Turn on the bus and logic analyzer.

The connectors on the HP 10343B are tied in parallel so that all the connectors and cable combinations can be used with a Single-Ended or Differential Bus. Also, there is always at least one connector that is not used. This connector may be used for additional analysis with an oscilloscope or other measurement device.

There are two connectors inside of the 10343B interface that can be reached by opening up the interface from the bottom of the HP 10269A/B. These connectors are the outputs of the input comparitors and may be used for looking at the SCSI Bus with an oscilloscope or other measurement device. These connectors are particularly useful for looking at the differential bus since their outputs give a single-ended representation of the bus. The outputs of the connectors are delayed from the actual bus by about 20 nanoseconds. These outputs are positive true on the HP 10343B, but are negative true on the SCSI bus.

Table 2-1 lists the HP 10343B connector part numbers and the part numbers for comparable cable connectors.

Table 2-1. Connector Part Numbers

HP 10343B Connector	Mating Connector	
(HP Part Number)	(3M Part Number*)	(AMP Part Number**)
1252-2076 (Nonshielded)	3425 Family	AMP 1-499206-0
1810-0272 (Shielded)	3564-1001	AMP 554216-1

*3M is a registered trademark of the Minnesota Mining and Manufacturing Company.

**AMP is a registered trademark of AMP Inc.

Selecting the Correct Inverse Assembler

The HP 10343B has ten inverse assemblers available for SCSI Bus system analysis. The interpretation of the SCSI command sets vary in each inverse assembler to match the applications of various device types. Only one inverse assembler can be used at a time.

Note

If you do not want to lose your current data, you must save your data before loading a different inverse assembler into the logic analyzer.

The inverse assemblers available are:

- ISCSIDIR
- ISCSISEQ
- ISCSIPTR
- ISCSIPRC
- ISCSISCN
- ISCSIDSE
- ISCSIAMC
- ISCSICOM
- ISCSIWRM
- ISCSIOPT

ISCSIDIR - Is for Direct Access Devices and Read Only Direct Access Devices.

ISCSISEQ - Is for Sequential Devices like tape backup drives.

ISCSIPTR - Is for Printers.

ISCSIPRC - Is for Processor Devices.

ISCSISCN - Is for Scanner Devices.

ISCSIDSE - Is a special application which is used when there is a Sequential Access Device on the SCSI Bus that uses Group 0 (6 byte) commands which communicates with a Direct Access Device that uses Group 1 (10 byte) commands.

ISCSIAMC - Is for Automatic Media Changers.

ISCSICOM - Is for Communication Devices.

ISCSIWRM - Is a special case inverse assembler designed for Write Once Read Multiple Devices. The following commands set it apart from ISCSIDIR.

- 15H Mode Select
- 1AH Mode Sense
- 28H Read
- 2EH Write and Verify
- 2FH Verify

ISCSIOPT - Is for Optical Memory Devices.

Refer to chapter 3 for more information on the inverse assemblers.

Note

For Read Only Direct Access Devices, ISCSIDIR should be used with the Group 0 (6 byte) commands and ISCSIWRM should be used with the Group 1 (10 byte) commands.

Loading an Inverse Assembler

To load an inverse assembler into the logic analyzer:

1. Connect the HP 9121D/S or HP 9122D/S 3.5 inch flexible disc drive to the logic analyzer.

2. Install the flexible disc labeled "HP 10343B Inverse Assemblers for use with HP 1630A/D/G and HP 1631A/D" in the HP 9121D/S or HP 9122D/S disc drive.

3. Select the SYSTEM menu of the logic analyzer and press the NEXT[ ] or PREV[ ] key until the [Storage Operations] menu is displayed.

4. Press INSERT to list the files on the disc.

5. Press the ROLL keys until the cursor (>) is next to the inverse assembler file that you want to load.

6. Select the Operation field with the CURSOR keys and press the NEXT[ ] or PREV[ ] key until the [Load] operation is displayed.

7. Press INSERT to load the file into the HP 1630A/D/G or HP 1631A/D Logic Analyzer.

Refer to chapter 3 for more information on the inverse assemblers.

Setting Up the Analyzer from the Disc

The logic analyzer must be configured for SCSI Bus analysis by loading the configuration file from the flexible disc after loading the inverse assembler file. To load the configuration file:

1. With the disc drive connected, install the flexible disc labeled "HP 10343B Inverse Assemblers for use with HP 1630A/D/G and HP 1631A/D" in the HP 9121D/S or HP 9122D/S disc drive.

2. Select the SYSTEM menu of the logic analyzer and press the NEXT[ ] or PREV[ ] key until the [Storage Operations] menu is displayed.

3. Select the [Storage Operations] field with the CURSOR keys and press INSERT to list the files on the disc.

4. Press the ROLL keys until the cursor (>) is next to the configuration file.

   - For the HP 1630A/D and HP 1631A/D, load the configuration file "CSCSICON."
   - For the HP 1630G, load the configuration file "CSCSICONG."

5. Select the Operation field with the CURSOR keys and press the NEXT[ ] or PREV[ ] key until the [Load] operation is displayed.

6. Press INSERT to load the file into the HP 1630A/D/G or HP 1631A/D Logic Analyzer.

Note

You must reload the configuration file into the analyzer everytime you load a different inverse assembler.

System Configuration

The System Configuration menu for an HP 1630D or HP 1631D Logic Analyzer is shown in figure 2-6. When an HP 1630A/G or HP 1631A is used, only eight timing channels are available.

Table 2-2 lists the SCSI signal connections for each pod.

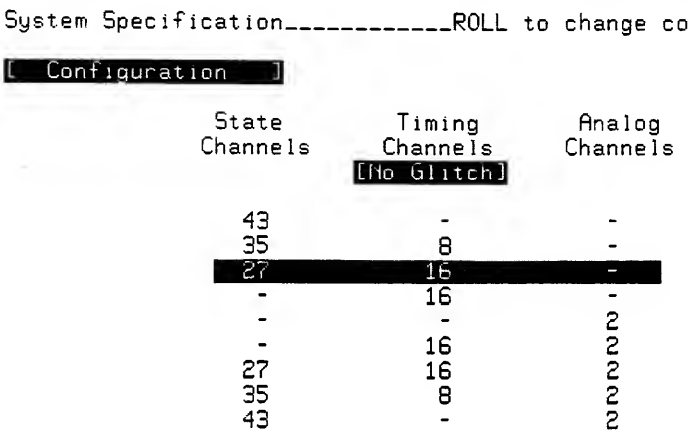


Figure 2-6. System Configuration Menu

Format Specification

The configuration files contain predefined format specifications (see figure 2-7). These specifications include all labels required for monitoring the SCSI Bus system. The Data- field lists the hexadecimal data that is interpreted by the inverse assembler in the Data field.

Note

ADDR is not used by the SCSI bus, but is required for inverse assembly.

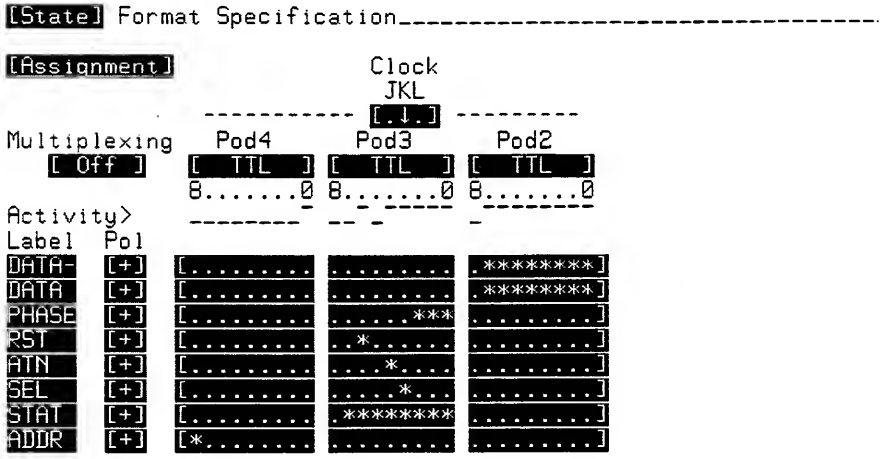


Figure 2-7. Format Specification

Symbols

The User Base menu of the format specification is set up with symbol names to identify commands, status conditions, messages, etc. (see figure 2-8).

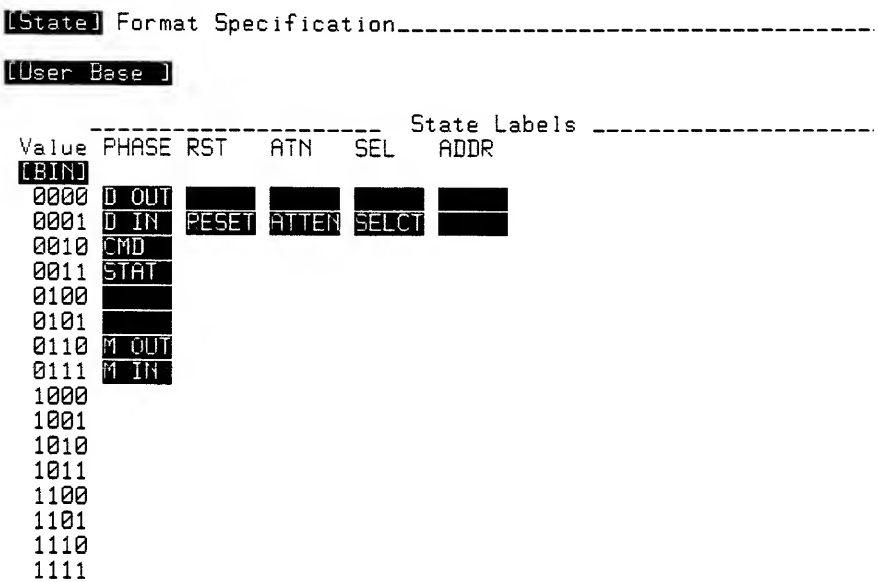


Figure 2-8. User Base Menu for the HP 10343B

Accumulating Data

Touch RUN and, as soon as there is activity on the bus, the logic analyzer will begin to accumulate data. The analyzer will continue to accumulate data and will display the data when the analyzer memory is full or when you touch STOP.

Note

The logic analyzer will flash "Warning Slow Clock" when data is no longer being transmitted across the bus.

Listing Menu

Captured data is displayed as shown in figure 2-9. The inverse assemblers are constructed so the output lists the actual commands, status conditions, messages, and phases of the SCSI Bus.

```
[State] Listing_____________________________________________
                                                          ←
Label> DATA-  Phase  SCSI mnemonic                        PHASE
Base > [HEX]  [                    HSM                 ] [ USR
[Mark]  XX    [      .          Instructions             ] [XXXXX

+0000*  01    Arbitr ID=0                                  D OUT
+0001*  02    Reslct Atn ID=1                              D IN
+0002*  C0    Msg_in Identify Disconnect Allowed Lu=0       M IN
+0003*  00    Commd  Test Unit Ready                       CMD
+0004*  1F    Commd  Lu=0                                  CMD
+0005   02    Commd                                        CMD
+0006   03    Commd                                        CMD
+0007   04    Commd                                        CMD
+0008   FF    Commd                                        CMD
+0009*  06    Commd  * PARITY ERROR *                      CMD
+0010*  0F    Commd  Rst Autosense Flag Link               CMD
+0011*  00    Status Rst Good                              STAT
+0012*  0E    Msgout Rst Reserved                          M OUT
+0013*  00    Reset Bus Free                               D OUT
```

Figure 2-9. Listing Menu for the SCSI Bus

Timing Analysis

Figure 2-10 lists the format specification for timing analysis. All of the SCSI lines can be seen on the HP 1630D and HP 1631D analyzer, but the Timing Selector Switch on the HP 10343B must be used to see the Parity, Select, or Reset line. Since the HP 1630A/G and HP 1631A Logic Analyzers have only eight timing channels, only the Timing Data or Status lines can be seen at one time with these analyzers. To look at the Status or Data lines, you must manually move pod 1 of the logic analyzer between connector C (Data) and connector D (Status) of the HP 10269A/B.

Table 2-2 lists the SCSI signal connections for each pod.

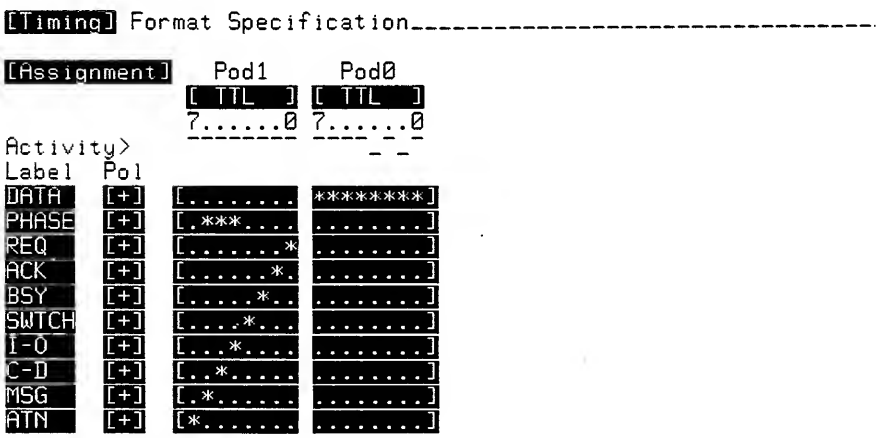


Figure 2-10. Format Specification for Timing

Signal Connections

The HP 10343B monitors all SCSI lines for state information. Eight or sixteen lines (depending on the analyzer) can be monitored for timing information. Table 2-2 lists the SCSI signals and connections for the HP 1630A/D/G and HP 1631A/D Logic Analyzers.

Table 2-2. Logic Analyzer to SCSI Signal Connections

Function / State	HP 1630A/G and HP 1631A		HP 1630D and HP 1631D	
	Pod	Bit	Pod	Bit
Data 0	2	0	2	0
Data 1	2	1	2	1
Data 2	2	2	2	2
Data 3	2	3	2	3
Data 4	2	4	2	4
Data 5	2	5	2	5
Data 6	2	6	2	6
Data 7	2	7	2	7
I/O	3	0	3	0
C/D	3	1	3	1
MSG	3	2	3	2
SEL	3	3	3	3
ATN	3	4	3	4
PARITY ERROR	3	5	3	5
RESET	3	6	3	6
INF	3	7	3	7

Table 2-2. Logic Analyzer to SCSI Signal Connections (Continued)

Function Timing	HP 1630A/G and HP 1631A		HP 1630D and HP 1631D	
	Pod	Bit	Pod	Bit
Data 0	1	0	0	0
Data 1	1	1	0	1
Data 2	1	2	0	2
Data 3	1	3	0	3
Data 4	1	4	0	4
Data 5	1	5	0	5
Data 6	1	6	0	6
Data 7	1	7	0	7
Request	1	0	1	0
Ack	1	1	1	1
Busy	1	2	1	2
Sel Sw	1	3	1	3
I/O	1	4	1	4
C/D	1	5	1	5
MSG	1	6	1	6
Atten	1	7	1	7

Note: Since only one pod (eight channels) are available for timing analysis on the HP 1630A/G and HP 1631A Logic Analyzers, only one group of timing lines (Data or Status) can be analyzed at one time.

LED Indicators

Two LED light bars of 10 LEDs each are used as front panel indicators for static conditions of the bus (see figure 2-11).

- One group for Data; and
- One group for Status.

For Data, data bits 0 through 7, Parity, and a Parity Error LED light is provided. The Parity Error is not one of the SCSI signal lines, but is generated by internal hardware of the interface when a parity error occurs and the front panel State Parity Error switch is on.

Note

There are two parity lights on the Data light bar. The Data Parity bit is part of the SCSI bus. The Parity Error is generated by the interface when there is an Odd Parity Error. This light comes on only if the Parity Selector Switch is on and a parity error is detected.

Nine SCSI Status lines are shown on the other LED light bar. These include I/O, C/D, MSG, and the SCSI phases.

Also, an internal line that is unique to the interface is on the tenth LED. This LED is labeled as INF for "Information Transfer." INF is on when the bus is in the Data, Command, Status, or Message phases and turns off when the bus goes into the Bus Free State. This indicator remains off during the Arbitration, Select, and Reselect phases.

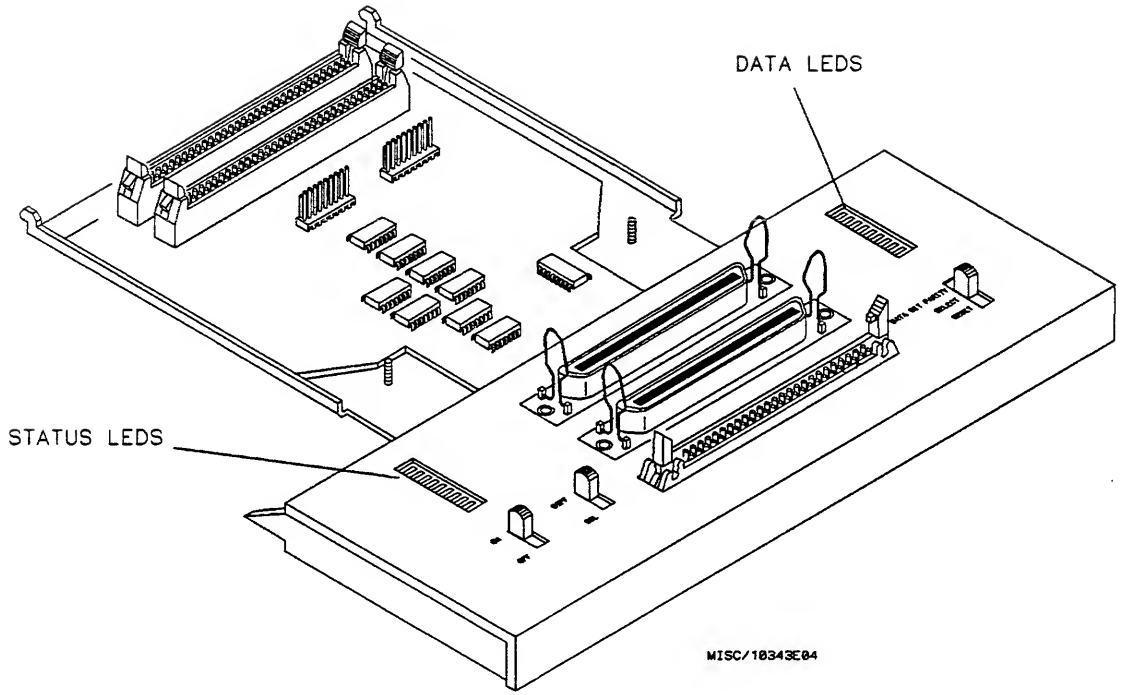


Figure 2-11. LED Locations

HP 10343B Inverse Assemblers 3

Introduction

The HP 10343B has ten inverse assemblers available for use with the HP 1630A/D/G and HP 1631A/D Logic Analyzers. These give you the flexiblity of selecting the correct inverse assembler to decode any of the different device types that are called out in the SCSI Standard X3T9.2/86-109 Revision 2.

The interpretation of the SCSI Command Sets vary in each inverse assembler to match the applications of various device types. Only one inverse assembler can be used at a time.

Selecting the Correct Inverse Assembler

The HP 1630A/D/G or HP 1631A/D Logic Analyzer is configured for SCSI Bus analysis by loading the appropriate inverse assembler and then loading the configuration file. Each time you load a new inverse assembler you must reload the configuration file.

Note

If you do not want to lose your current data, you must save your data before loading a different inverse assembler into the logic analyzer.

The inverse assemblers available are:

- ISCSIDIR
- ISCSISEQ
- ISCSIPTR
- ISCSIPRC
- ISCSISCN
- ISCSIDSE
- ISCSIAMC
- ISCSICOM
- ISCSIWRM
- ISCSIOPT

ISCSIDIR - Is for Direct Access Devices and Read Only Direct Access Devices.

ISCSISEQ - Is for Sequential Devices like tape backup drives.

ISCSIPTR - Is for Printers.

ISCSIPRC - Is for Processor Devices.

ISCSISCN - Is for Scanner Devices.

ISCSIDSE - Is a special application which is used when there is a Sequential Access Device on the SCSI Bus that uses the Group 0 (6 byte) commands which communicate with a Direct Access Device that uses Group 1 (10 byte) commands.

ISCSIAMC - Is for Automatic Media Changers.

ISCSICOM - Is for Communication Devices.

ISCSIWRM - Is a special case inverse assembler designed for Write Once Read Multiple Devices. The following commands set it apart from ISCSIDIR.

- 15H Mode Select
- 1AH Mode Sense
- 28H Read
- 2EH Write and Verify
- 2FH Verify

ISCSIOPT - Is for Optical Memory Devices.

Note

For Read Only Direct Access Devices, "ISCSIDIR" should be used with the Group 0 (6 byte) commands and "ISCSIWRM" should be used with Group 1 (10 byte) commands.

There is a good possibility that your SCSI Bus system will be made up of several different device types. Often, even the initiator and the target may be different device types. In this situation you may need to decide which inverse assembler will best fit your needs. To make it easier to select the appropriate inverse assembler, the commands for each device type are listed in tables 3-1 through 3-10. By comparing the commands for each inverse assembler, the most appropriate inverse assembler can be selected.

Table 3-1. ISCSIDIR Commands

Group 0 Commands (6 byte)	Group 1 Commands (10 byte)	Group 5 Commands (12 byte)
00 Test Unit Ready	24 Define Window	A5 Move Medium
01 Rezero	25 Read Capacity	A6 Exchange Medium
03 Request Sense	28 Read X	A8 Read
04 Format Unit	2A Write X	AA Write
05 Read Block Limits	2B Seek X	AC Erase
07 Reassign Block	2C Erase	AE Write and Verify
08 Read	2D Read Update Block	AF Verify
0A Write	2E Write and Verify	
0B Seek	2F Verify	
0F Read Reverse	30 Search High	
10 Write Filemarks	31 Search =	
11 Space	32 Search Low	
12 Enquiry	33 Set Limits	
13 Verify	34 Pre-Fetch	
14 Recovered Buffer	35 Flush Cache	
15 Mode Select	36 Lock/Unlock Cache	
16 Reserve	37 Read Defect Data	
17 Release	39 Compare	
18 Copy	3A Copy and Verify	
19 Erase	3B Write Buffer	
1A Mode Sense	3C Read Buffer	
1B Start/Stop	3D Update Block	
1C Receive Diagnostics	3E Read Long	
1D Send Diagnostics	3F Write Long	
1E Prevent/Allow		
1F Read Log		

Table 3-2. ISCSISEQ Commands

Group 0 Commands (6 byte)	Group 1 Commands (10 byte)	Group 5 Commands (12 byte)
00 Test Unit Ready	24 Define Window	A5 Move Medium
01 Rewind	25 Read Capacity	A6 Exchange Medium
03 Request Sense	28 Read X	A8 Read
04 Format Unit	2A Write X	AA Write
05 Read Block Limits	2B Locate	AC Erase
07 Reassign Block	2C Erase	AE Write and Verify
08 Read	2D Read Update Block	AF Verify
0A Write	2E Write and Verify	
0B Track Select	2F Verify	
0F Read Reverse	30 Search High	
10 Write Filemarks	31 Search =	
11 Space	32 Search Low	
12 Enquiry	33 Set Limits	
13 Verify	34 Read Position	
14 Recovered Buffer	35 Flush Cache	
15 Mode Select	36 Lock/Unlock Cache	
16 Reserve	37 Read Defect Data	
17 Release	39 Compare	
18 Copy	3A Copy and Verify	
19 Erase	3B Write Buffer	
1A Mode Sense	3C Read Buffer	
1B Load/Unload	3D Update Block	
1C Receive Diagnostics	3E Read Long	
1C Send Diagnostics	3F Write Long	
1D Prevent/Allow		
1F Read Log		

Table 3-3. ISCSIPTR Commands

Group 0 Commands (6 byte)	Group 1 Commands (10 byte)	Group 5 Commands (12 byte)
00 Test Unit Ready	24 Define Window	A5 Move Medium
01 Rezero	25 Read Capacity	A6 Exchange Medium
03 Request Sense	28 Read X	A8 Read
04 Format Unit	2A Write X	AA Write
05 Read Block Limits	2B Seek X	AC Erase
07 Reassign Block	2C Erase	AE Write and Verify
08 Read	2D Read Update Block	AF Verify
0A Print	2E Write and Verify	
0B Slew and Print	2F Verify	
0F Read Reverse	30 Search High	
10 Flush Buffer	31 Search =	
11 Space	32 Search Low	
12 Inquiry	33 Set Limits	
13 Verify	34 Pre-Fetch	
14 Recovered Buffer	35 Flush Cache	
15 Mode Select	36 Lock/Unlock Cache	
16 Reserve	37 Read Defect Data	
17 Release	39 Compare	
18 Copy	3A Copy and Verify	
19 Erase	3B Write Buffer	
1A Mode Sense	3C Read Buffer	
1B Stop Print	3D Update Block	
1C Receive Diagnostics	3E Read Long	
1D Send Diagnostics	3F Write Long	
1E Prevent/Allow		
1F Read Log		

Table 3-4. ISCSIPRC Commands

Group 0 Commands (6 byte)	Group 1 Commands (10 byte)	Group 5 Commands (12 byte)
00 Test Unit Ready	24 Define Window	A5 Move Medium
01 Rezero	25 Read Capacity	A6 Exchange Medium
03 Request Sense	28 Read X	A8 Read
04 Format Unit	2A Write X	AA Write
05 Read Block Limits	2B Seek X	AC Erase
07 Reassign Block	2C Erase	AE Write and Verify
08 Receive	2D Read Update Block	AF Verify
0A Send	2E Write and Verify	
0B Seek	2F Verify	
0F Read Reverse	30 Search High	
10 Write Filemarks	31 Search =	
11 Space	32 Search Low	
12 Inquiry	33 Set Limits	
13 Verify	34 Pre-Fetch	
14 Recovered Buffer	35 Flush Cache	
15 Mode Select	36 Lock/Unlock Cache	
16 Reserve	37 Read Defect Data	
17 Release	39 Compare	
18 Copy	3A Copy and Verify	
19 Erase	3B Write Buffer	
1A Mode Sense	3C Read Buffer	
1B Start/Stop	3D Update Block	
1C Receive Diagnostics	3E Read Long	
1D Send Diagnostics	3F Write Long	
1E Prevent/Allow		
1F Read Log		

Table 3-5. ISCSISCN Commands

Group 0 Commands (6 byte)	Group 1 Commands (10 byte)	Group 5 Commands (12 byte)
00 Test Unit Ready	24 Define Window	A5 Move Medium
01 Rezero	25 Get Window	A6 Exchange Medium
03 Request Sense	28 Read X	A8 Read
04 Format Unit	2A Send X	AA Write
05 Read Block Limits	2B Seek X	AC Erase
07 Reassign Block	2C Erase	AE Write and Verify
08 Read	2D Read Update Block	AF Verify
0A Write	2E Write and Verify	
0B Seek	2F Verify	
0F Read Reverse	30 Search High	
10 Write Filemarks	31 Medium Position	
11 Space	32 Search Low	
12 Inquiry	33 Set Limits	
13 Verify	34 Get Status	
14 Recovered Buffer	35 Flush Cache	
15 Mode Select	36 Lock/Unlock Cache	
16 Reserve	37 Read Defect Data	
17 Release	39 Compare	
18 Copy	3A Copy and Verify	
19 Erase	3B Write Buffer	
1A Mode Sense	3C Read Buffer	
1B Scan	3D Update Block	
1C Receive Diagnostics	3E Read Long	
1D Send Diagnostics	3F Write Long	
1E Prevent/Allow		
1F Read Log		

Table 3-6. ISCSIDSE Commands

Group 0 Commands (6 byte)	Group 1 Commands (10 byte	Group 5 Commands (12 byte)
00 Test Unit Ready	24 Define Window	A5 Move Medium
01 Rewind	25 Read Capacity	A6 Exchange Medium
03 Request Sense	28 Read X	A8 Read
04 Format Unit	2A Write X	AA Write
05 Read Block Limits	2B Seek X	AC Erase
07 Reassign Block	2C Erase	AE Write and Verify
08 Read	2D Read Update Block	AF Verify
0A Write	2E Write and Verify	
0B Track Select	2F Verify	
0F Read Reverse	30 Search High	
10 Write Filemarks	31 Search =	
11 Space	32 Search Low	
12 Inquiry	33 Set Limits	
13 Verify	34 Pre-Fetch	
14 Recovered Buffer	35 Flush Cache	
15 Mode Select	36 Lock/Unlock Cache	
16 Reserve	37 Read Defect Data	
17 Release	39 Compare	
18 Copy	3A Copy and Verify	
19 Erase	3B Write Buffer	
1A Mode Sense	3C Read Buffer	
1B Load/Unload	3D Update Block	
1C Receive Diagnostics	3E Read Long	
1D Send Diagnostics	3F Write Long	
1E Prevent/Allow		
1F Read Log		

Table 3-7. ISCSIAMC Commands

Group 0 Commands (6 byte)	Group 1 Commands (10 byte)	Group 5 Commands (12 byte)
01 Rezero	24 Define Window	A5 Move Medium
03 Request Sense	25 Read Capacity	A6 Exchange Medium
04 Format Unit	28 Read X	A8 Read
05 Read Block Limits	2A Write X	AA Write
07 Reassign Block	2B Seek X	AC Erase
08 Read	2C Erase	AE Write and Verify
0A Write	2D Read Update Block	AF Verify
0B Seek	2E Write and Verify	
0F Read Reverse	2F Verify	
10 Write Filemarks	30 Search High	
11 Space	31 Search =	
12 Inquiry	32 Search Low	
13 Verify	33 Set Limits	
14 Recovered Buffer	34 Pre-Fetch	
15 Mode Select	35 Flush Cache	
16 Reserve	36 Lock/Unlock Cache	
17 Release	37 Read Defect Data	
18 Copy	38 Read Element Status	
19 Erase	39 Compare	
1A Mode Sense	3A Copy and Verify	
1B Start/Stop	3B Write Buffer	
1C Receive Diagnostics	3C Read Buffer	
1D Send Diagnostics	3D Update Block	
1E Prevent/Allow	3E Read Long	
1F Read Log		
3F Write Long		

Table 3-8. ISCSICOM Commands

Group 0 Commands (6 byte)	Group 1 Commands (10 byte)	Group 5 Commands (12 byte)
01 Rezero	24 Define Window	A5 Move Medium
03 Request Sense	25 Read Capacity	A6 Exchange Medium
04 Format Unit	28 Read X	A8 Read
05 Read Block Limits	2A Write X	AA Write
07 Reassign Block	2B Seek X	AC Erase
08 Get Message	2C Erase	AE Write and Verify
0A Send Message	2D Read Update Block	AF Verify
0B Seek	2E Write and Verify	
0F Read Reverse	2F Verify	
10 Write Filemarks	30 Search High	
11 Space	31 Search =	
12 Inquiry	32 Search Low	
13 Verify	33 Set Limits	
14 Recovered Buffer	34 Pre-Fetch	
15 Mode Select	35 Flush Cache	
16 Reserve	36 Lock/Unlock Cache	
17 Release	37 Read Defect Data	
18 Copy	39 Compare	
19 Erase	3A Copy and Verify	
1A Mode Sense	3B Write Buffer	
1B Start/Stop	3C Read Buffer	
1C Receive Diagnostics	3D Update Block	
1D Send Diagnostics	3E Read Long	
1E Prevent/Allow	3F Write Long	
1F Read Log		

Table 3-9. ISCSIWRM Commands

Group 0 Commands (6 byte)	Group 1 Commands (10 byte)	Group 5 Commands (12 byte)
01 Rezero	24 Define Window	A5 Move Medium
03 Request Sense	25 Read Capacity	A6 Exchange Medium
04 Format Unit	28 Read X	A8 Read
05 Read Block Limits	2A Write X	AA Write
07 Reassign Block	2B Seek X	AC Erase
08 Read	2C Erase	AE Write and Verify
0A Write	2D Read Update Block	AF Verify
0B Seek	2E Write and Verify	
0F Read Reverse	2F Verify	
10 Write Filemarks	30 Search High	
11 Space	31 Search =	
12 Inquiry	32 Search Low	
13 Verify	33 Set Limits	
14 Recovered Buffer	34 Pre-Fetch	
15 Mode Select	35 Flush Cache	
16 Reserve	36 Lock/Unlock Cache	
17 Release	37 Read Defect Data	
18 Copy	39 Compare	
19 Erase	3A Copy and Verify	
1A Mode Sense	3B Write Buffer	
1B Start/Stop	3C Read Buffer	
1C Receive Diagnostics	3D Update Block	
1D Send Diagnostics	3E Read Long	
1E Prevent/Allow	3F Write Long	
1F Read Log		

Table 3-10. ISCSIOPT Commands

Group 0 Commands (6 byte)	Group 1 Commands (10 byte)	Group 5 Commands (12 byte)
01 Rezero	24 Define Window	A5 Move Medium
03 Request Sense	25 Read Capacity	A6 Exchange Medium
04 Format Unit	28 Read X	A8 Read
05 Read Block Limits	2A Write X	AA Write
07 Reassign Block	2B Seek X	AC Erase
08 Read	2C Erase	AE Write and Verify
0A Write	2D Read Update Block	AF Verify
0B Seek	2E Write and Verify	
0F Read Reverse	2F Verify	
10 Write Filemarks	30 Search High	
11 Space	31 Search =	
12 Inquiry	32 Search Low	
13 Verify	33 Set Limits	
14 Recovered Buffer	34 Pre-Fetch	
15 Mode Select	35 Flush Cache	
16 Reserve	36 Lock/Unlock Cache	
17 Release	37 Read Defect Data	
18 Copy	38 Media Scan	
19 Erase	39 Compare	
1A Mode Sense	3A Copy and Verify	
1B Start/Stop	3B Write Buffer	
1C Receive Diagnostics	3C Read Buffer	
1D Send Diagnostics	3D Update Block	
1E Prevent/Allow	3E Read Long	
1F Read Log	3F Write Long	

Loading a Different Inverse Assembler

To load a different inverse assembler:

1. Connect the HP 9121D/S or HP 9122D/S 3.5-inch flexible disc drive to the logic analyzer.

2. Install the flexible disc labeled "HP 10343B Inverse Assemblers for use with HP 1630A/D/G and HP 1631A/D" in the HP 9121D/S or HP 9122D/S disc drive.

3. Select the SYSTEM menu of the logic analyzer and press the NEXT[ ] or PREV[ ] key until the [Storage Operations] menu is displayed.

4. Press INSERT to list the files on the disc.

5. Press the ROLL keys until the cursor (>) is next to the inverse assembler file you want to load.

6. Select the Operation field with the CURSOR keys and press the NEXT[ ] or PREV[ ] key until the [Load] operation is displayed.

7. Press INSERT to load the file into the HP 1630A/D/G or HP 1631A/D Logic Analyzer.

Note

The configuration file "CSCSICON" must be reloaded each time you load a different inverse assembler file.

8. Press the ROLL keys until the cursor (>) is next to the configuration file "CSCSICON."

9. Select the Operation field with the CURSOR keys and press the NEXT[ ] or PREV[ ] key until the [Load] operation is displayed.

10. Press INSERT to load the configuration file into the HP 1630A/D/G or HP 1631A/D Logic Analyzer.

Inverse Assembly Operation

The HP 10343B inverse assemblers are designed to decode commands, messages, phases, and status conditions for 8-Bit Single-Ended and Differential SCSI Bus systems. Rolling the screen up will inverse assemble the lines as they appear on the bottom of the screen. If you jump to another area of the screen by entering a new line number, simply roll the screen up to inverse assemble that block of memory.

Note

Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but the activity between those blocks will not be inverse assembled.

Also, blocks may not be correctly inverse assembled if you roll the screen down, scrolling information from the top of the screen to the bottom. To correctly inverse assemble these blocks, simply move the first line of interest off the bottom of the screen and roll the screen up.

Each line of the inverse assembler listing is identified by type: Command, Status, etc. Figure 3-1 shows an example of an HP 10343B inverse assembly listing.

```
[State] Listing_____________________________________________________
                                                                    ←
Label> DATA-  Phase  SCSI mnemonic                                PHASE
Base > [HEX]  [                    ASM                          ] [ USR
[Mark] XX     [                 Instructions                    ] [XXXXX

+0000*  01    Arbitr ID=0                                         D OUT
+0001*  02    Reslct Atn ID=1                                     D IN
+0002*  C0    Msg_in Identify Disconnect Allowed Lu=0             M IN
+0003*  00    Commd  Test Unit Ready                              CMD
+0004*  1F    Commd  Lu=0                                         CMD
+0005   02    Commd                                               CMD
+0006   03    Commd                                               CMD
+0007   04    Commd                                               CMD
+0008   FF    Commd                                               CMD
+0009*  06    Commd  * PARITY ERROR *                             CMD
+0010*  0F    Commd  Rst Autosense Flag Link                      CMD
+0011*  00    Status Rst Good                                     STAT
+0012*  0E    Msgout Rst Reserved                                 M OUT
+0013*  00    Reset Bus Free                                      D OUT
```

Figure 3-1. Inverse Assembler Listing

Interpreting Commands

The HP 10343B inverse assemblers decode six, ten, and twelve byte commands. The first line of the command lists the block address of the command, the actual command, and the length of the block. The second line lists the logical unit of the selected peripheral device and lists the names of any states that are true (logical 1). For example, byte 1 of a command often has bit 4 as DPO, bit 3 as FUA, and bit 1 as RelAdr. If all three of these bits were set as true, the following information would be displayed on the second line:

```
DPO FUA RelAdr
```

The last line lists the Autosense flag and link conditions when they are true (logical 1).

Tables 3-1 through 3-10 list the commands supported by the HP 10343B inverse assemblers.

Interpreting Vender Unique and Reserved Information

The SCSI Standard X3T9.2/86-109 Revision 2 has set aside some of the byte assignments for messages, status, and commands as either reserved for later definition or vendor unique. In the case of message and status, the HP 10343B inverse assembler listing will display the hexadecimal code for the information, list the information as either a message or status, and indicate if the information is vender unique or reserved.

For commands, the HP 10343B inverse assembler listing will display the hexadecimal code for the command, list the information as a command, and indicate which group the command is from.

Interpreting Messages

The HP 10343B inverse assemblers decode the name of the message on the first line and indicate whether the message is going into the initiator (Msg_in) or out of the initiator (Msgout). The messages supported by the HP 10343B are:

- 00h Command Complete
- 01h Extended Message
- 02h Save Data Pointer
- 03h Restore Pointers
- 04h Disconnect
- 05h Initiator Detected Error
- 06h Abort
- 07h Message Reject
- 08h No Operation
- 09h Message Parity Error
- 0Ah Linked Command Complete
- 0Bh Linked Command Complete (with Flag)
- 0Ch Bus Device Reset
- 0Dh Autosense Data Follows
- 0Eh - 7Fh Reserved Codes
- 80h - FFh Identify

Note

Identify messages include a logic unit specifier.

Extended Messages. Most messages are only one byte long, but extended messages may be up to 256 bytes long. When the HP 10343B inverse assemblers decode an extended message, the name of the message is shown on the first line along with "xmsg" to identify it as an extended message. Also, Msg_in or Msgout appears on the first line to indicate whether the message is going into the initiator or out of the initiator.

Each extended message will also include information specific to that message on the first line:

- Modify Data Pointer includes the message arguments;
- Synchronous Data Transfer Request includes the transfer period and offset as a hexadecimal byte;
- Extended Identify includes a logical unit number; and
- Wide Data Transfer Request includes the transfer width as a hexadecimal byte.

The next line shows the length of the extended message in hexadecimal and the third line lists the message code. For a complete description of specific extended messages, refer to the SCSI Standard X3T9.2/86-109 Revision 2.

Interpreting Status

The HP 10343B inverse assemblers decode all status conditions. Since status is only one byte, the actual status is listed following the status identifier. The status values supported by the HP 10343B inverse assemblers are:

- Good
- Check Condition
- Condition Met/Good
- Reserved
- Busy
- Intermediate/Good
- Intermediate/Condition Met/Good
- Reservation Conflict

For more information, refer to the SCSI Standard X3T9.2/86-109 Revision 2.

Interpreting Data

Since the data going across the bus is totally dependent and defined by the user, the HP 10343B inverse assemblers can only indicate whether the data is going into the initiator (Dat_in) or out of the initiator (Datout). The rest of the information cannot be interpreted by the HP 10343B.

Arbitration, Select, and Reselect Phases

When an Arbitration, Select, or Reselect phase occurs, the HP 10343B inverse assemblers identify the phase and list the interface device that is involved. For example:

```
Arbitr ID=3
```

indicates that interface device 3 has started an Arbitration phase.

Attention and Reset

The HP 10343B inverse assemblers will display the Attention bit (Atn) for every state in which the Attention bit is asserted true.

Likewise, the Reset bit (Rst) will be displayed for every state where it is asserted true. If the Reset bit becomes true while the SCSI bus is in the Bus Free state, the state is interpreted as "Reset Bus Free." If the Reset bit is true as the bus enters the Bus Free state, the state is also interpreted as "Reset Bus Free."

Parity Error

When the inverse assembler detects a parity error, it stops inverse assembly until the next valid state and displays "* PARITY ERROR *."

If a parity error is detected on the first line of a command, status, or message, then that line is not decoded. If the parity error is detected after the first line, the command or message is decoded.

Note

If parity is selected for the HP 10343B and parity is not used in your SCSI Bus system, excess parity errors will appear on the listing display.

Additional Information A

Introduction

This appendix contains information about the hardware supplied with the HP 10343B Bus Preprocessor, including a list of specifications and characteristics, and an overview of the theory of operation.

Specifications and Characteristics

Bus Compatibility: 8-Bit Single-Ended and Differential SCSI Bus systems containing any of the device types specified in the SCSI Standard X3T9.2/86-109 Revision 2.

SCSI Standard Supported: X3T9.2/86-109 Revision 2.

SCSI Device Types Supported:
ISCSIDIR - Direct Access Devices
ISCSISEQ - Sequential Devices
ISCSIPTR - Printers
ISCSIPRC - Processor Devices
ISCSISCN - Scanner Devices
ISCSIDSE - Sequential Devices using Group 0 (6 byte) commands communicating with a Direct Access Device using Group 1 (10 byte) commands.
ISCSIAMC - Automatic Media Changers
ISCSICOM - Communication Devices
ISCSIWRM - Write Once Read Multiple Devices
ISCSIOPT - Optical Devices

Accessories Required: HP 10343B and HP 10269A/B.

Maximum Data Rates:	10 Megabytes per second	

Note

Although the SCSI standard specifies the bus at 5.5 Megabytes per second, the HP 10343B is tested at 20 Megabytes per second using the Request and Acknowledge handshake lines.

Arbitration:	Setup Time:	30 ns
	Hold Time:	10 ns
Reselect/Select:	Setup Time:	30 ns
	Hold Time:	10 ns
Request Handshake Lines:	Setup Time:	30 ns
	Hold Time:	10 ns
Acknowledge Handshake Lines:	Setup Time:	30 ns
	Hold Time:	10 ns
Minimum Request and Acknowledge Pulse Width:	25 ns	

Note

SCSI lines are sampled 45 ns after Reset occurs during a Bus Free state.

Signal Line Loading:	0.4 mA TTL Low at 0.5 V.

Bus Cycles Interpreted:	Select/Reselect Arbitration Commands Messages Status Reset during a Bus Free State	
Power Requirements:	0.80 A at +5 Vdc max, supplied by the logic analyzer.	
Logic Analyzer Required:	HP 1630A/D/G, HP 1631A/D	
Number of Probes Used:	4 for HP 1630D and HP 1631D 3 for HP 1630A/G and HP 1631A	
Environmental Temperature:	Operating:	0 to +55 degrees C (+32 to +131 degrees F)
	Nonoperating:	-40 to +75 degrees C (-40 to +167 degrees F)
Altitude:	Operating:	4600 m (15,000 ft)
	Nonoperating:	15,300 m (50,000 ft)
Humidity:	To 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.	

Interface Description

The HP 10343B provides a complete mechanical and electrical interface between the HP 1630A/D/G or HP 1631A/D and your 8 Bit SCSI Bus system. This interface allows the logic analyzer to capture and decode all of the activaties on the SCSI bus. The SCSI bus is detected by high impedence comparitors on the HP 10343B. The outputs of these comparitors go directly to the logic analyzer for timing analysis.

For state analysis, the SCSI phase activities are decoded by the Phase Detection Logic. The logic analyzer clock is sent out at the correct times to capture the data.

Figure A-1 is a block diagram of the HP 10343B.

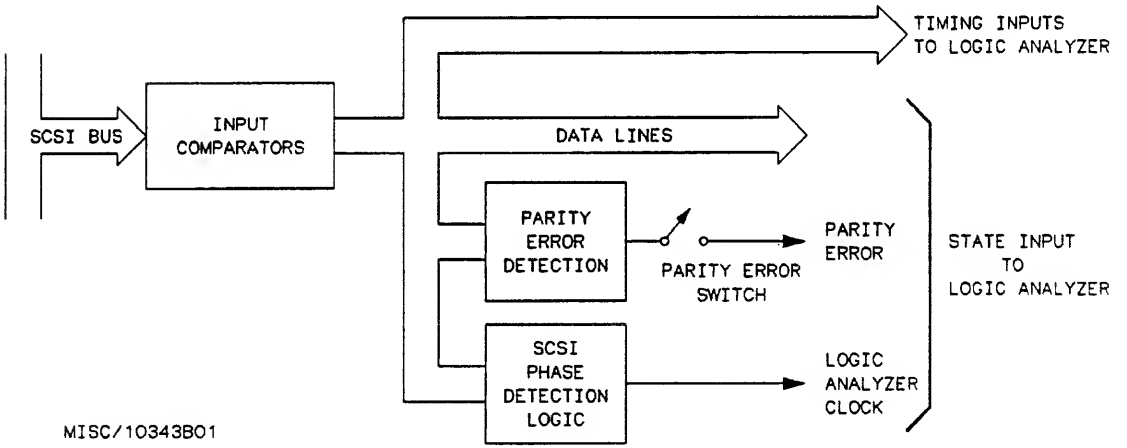


Figure A-1. HP 10343B Block Diagram

Theory of Operation

The inputs of the HP 10343B are received by two banks of analog comparitors (AM26LS32) on each line of the SCSI Bus. One bank of comparitors is used to receive single-ended signals and the other bank is used to recieve differential signals. U24 generates a 1.6 volt threshold level for single-ended signals. When operating in the single-ended mode, all SCSI devices ground the odd numbered pins. However, these pins are not grounded in the HP 10343B. Instead, the odd numbered pins are tied through the HP 10343B to the other SCSI connectors on the HP 10343B.

The two comparitors in parellel look like 5k ohms tied to a 2.5 volt source. A current of 420 uA is drawn from each line when the line is at a TTL Low of 0.4 volts. This is the active state of a line for a Single-Ended bus. The Differential bus will see a smaller load because its signals move between 2 and 3 volts.

Note

The term "active" and "released" are terms used in the SCSI Standard. "Active" is when the SCSI Bus goes true. In the Single-Ended Mode, this is when a line goes low on the SCSI Bus. Internally, after the input comparators on the HP 10343B interface board, "active" means a TTL high state. "Released" is a false or a high state on the SCSI bus, but on the interface board it is TTL low. This section uses the terms "active" and "released" in reference to the TTL levels on the interface board.

The selection of single-ended or differential bus is accomplished by enabling the output of one of the banks of comparitors with switch S1. The outputs of the comparitors are tristate. The SCSI Bus is low true, but the outputs of the input comparitors are positive true.

The comparitor outputs are connected directly to the interface output connectors J3 and J4. Through these connections the logic analyzer has a direct connection to the SCSI Bus.

Parity check is accomplished with U3. U3 is tied to the data lines DB0 through DB7 and DBP (Parity). The output of U3 is run through parity switch S2 so that this signal may be switched off when the SCSI Bus isn't using parity.

The output of the parity device U3 goes high if odd parity is not met. A high output is considered an error condition and is displayed on the logic analyzer screen as a "* PARITY ERROR *" when S2 is turned on.

All of the SCSI Bus lines are connected to LED indicators to allow the user to view the status condition of the SCSI Bus at a glance. These LED's are driven with open collector buffers U2, U21, U22, and Q1.

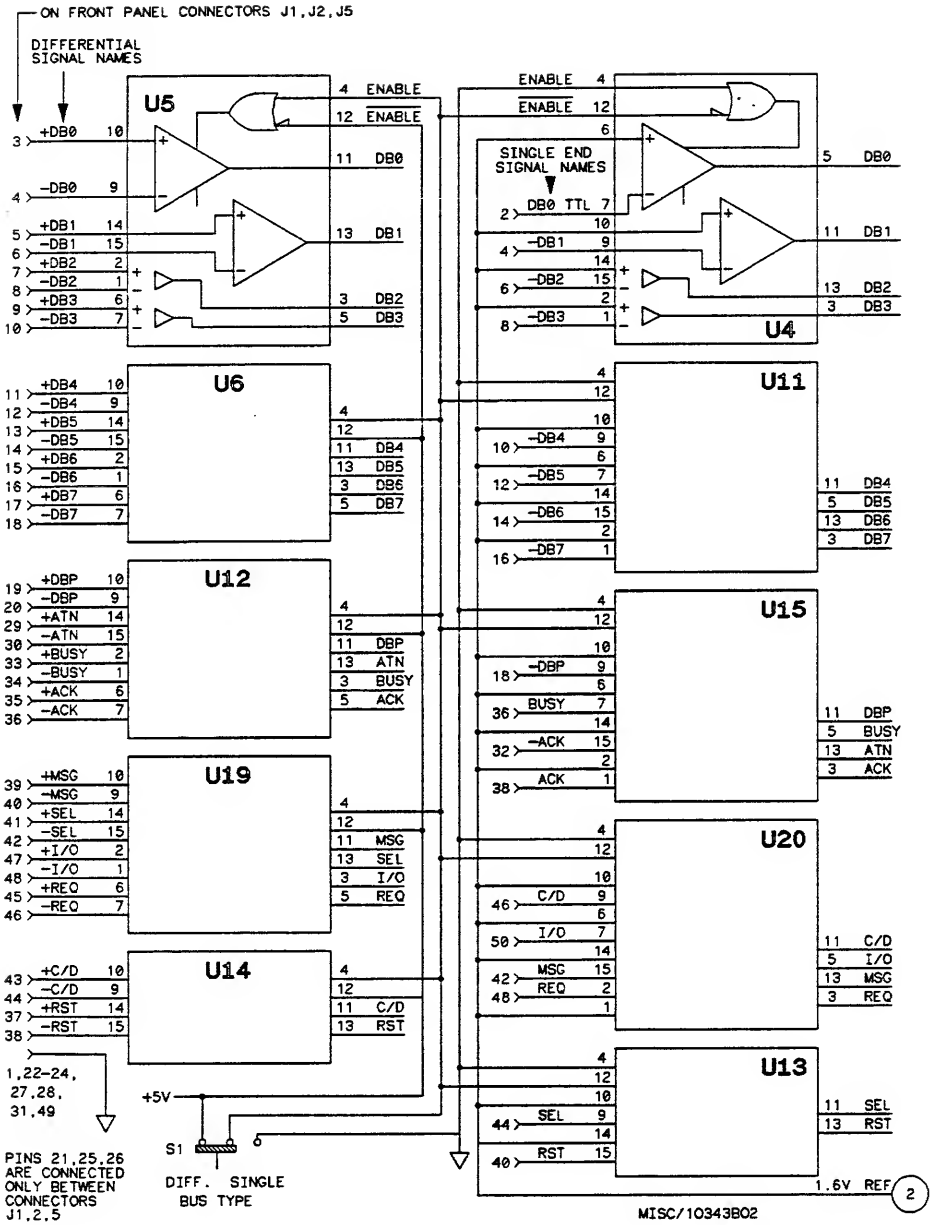


Figure A-2. HP 10343B Schematic

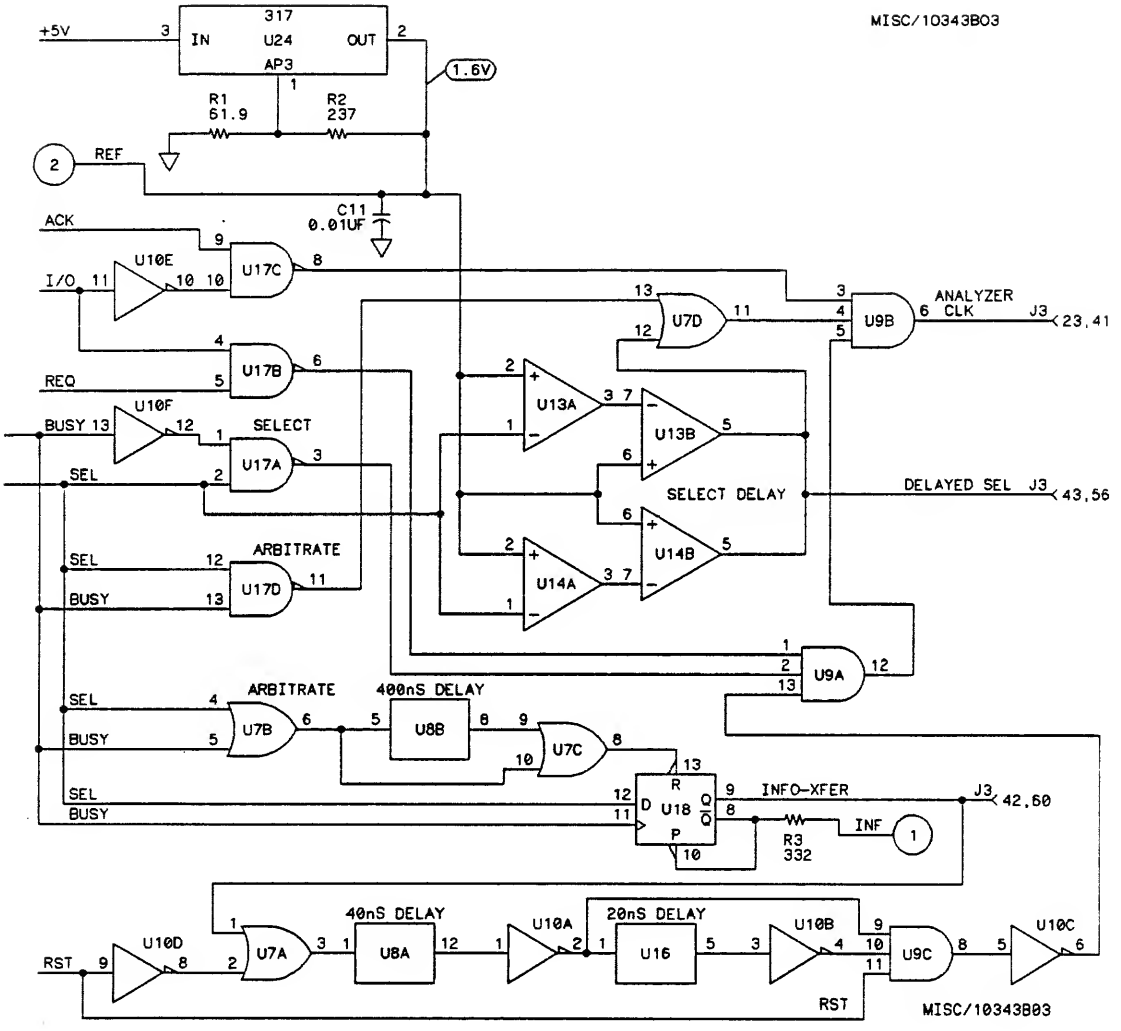


Figure A-2. HP 10343B Schematic (Continued)

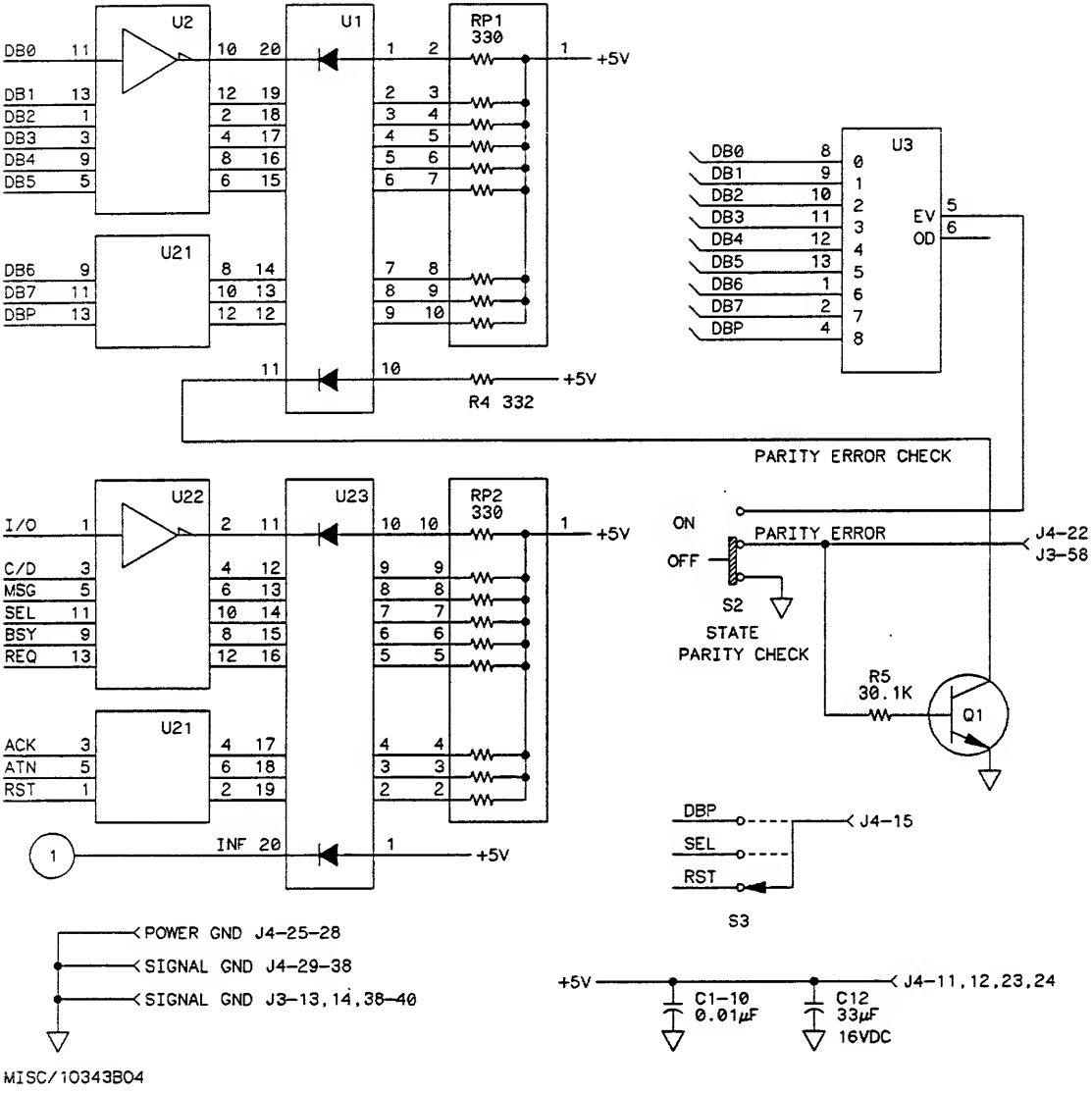
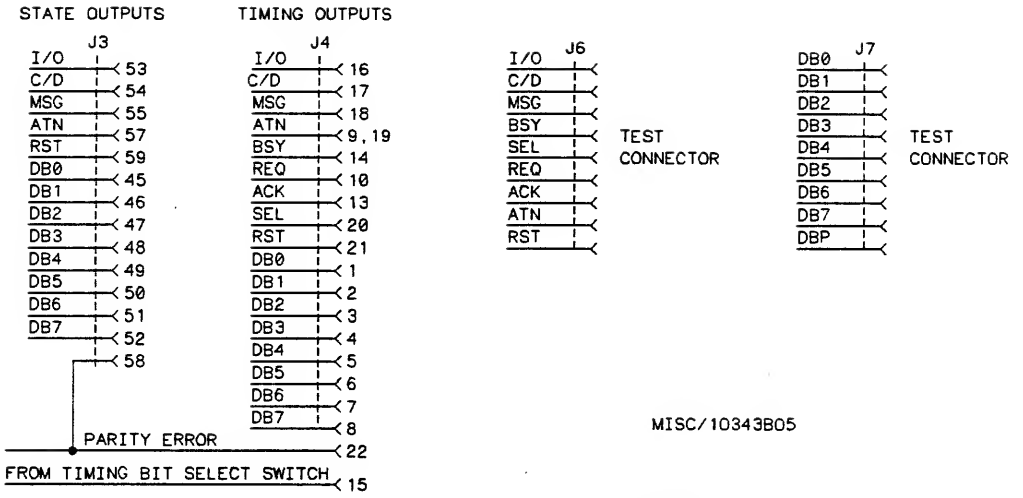


Figure A-2. HP 10343B Schematic (Continued)



*** * * * * * NOTICE * * * * * ***

The schematic on pages A-7 through A-10 is supplied only as an aid to understanding circuit interface characteristics. It is not intended to be used as a service or troubleshooting aid. This schematic is NOT subject to a revision or change program to keep it current or accurate. ACCORDINGLY, HEWLETT-PACKARD SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY ARISING FROM THE USE OF THIS SCHEMATIC.

Figure A-2. HP 10343B Schematic (Continued)

Generation of the Logic Analyzer Clocks

The logic analyzer stores the state of the data and status lines whenever it receives the falling edge of its clock. Setup and Hold times are referenced to this falling edge. There are four conditions in which the logic analyzer receives a clock:

- Arbitration phase;
- Select or Reselect phase;
- Information phase that is sent with handshake lines; and
- When Reset and Bus Free occurs at the same time.

Arbitration Phase. The analyzer clock gets a negative transition when both the Busy and Select lines go active, ending the SCSI Arbitration phase. This is accomplished with the NAND Gate U17D. The clock pulse is a 40nS pulse that is generated with the delay through the comparitors U13A/B or U14A/B, depending on whether the Single-ended or Differential mode is selected.

Select or Reselect Phase. The analyzer clock for the Select or Reselect phase is generated by Busy being low and Select being active or high. This is accomplished with the AND Gate U17A and by inverting Busy with U10F.

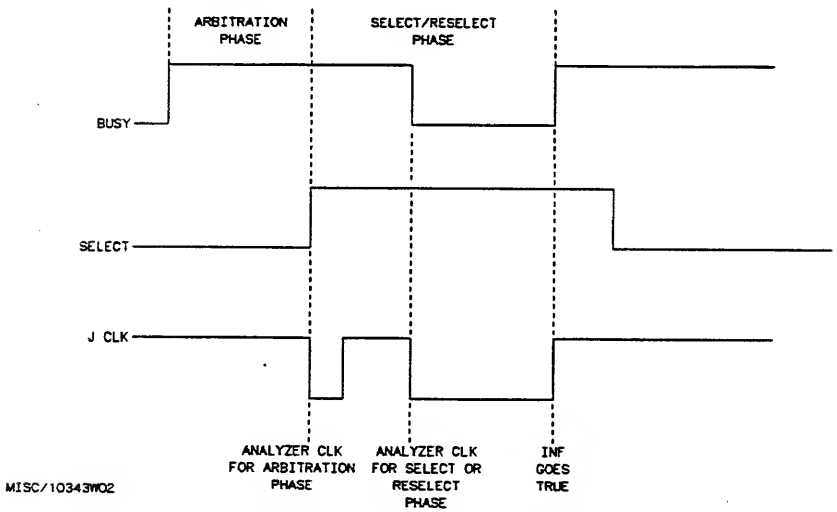


Figure A-3. HP 10343B Timing

Information Phase. When the SCSI Bus is transferring data and instructions, the handshake lines determine the clock. The I/O line determines which line, request or acknowledge, marks the data and status as valid. When the I/O line is asserted, the analyzer is clocked on the positive edge of the request line that comes from the comparitor into U17B. When the I/O line is not asserted it is inverted with U10E which then enables the NAND Gate U17C. This causes the acknowledge line to generate the analyzer clock.

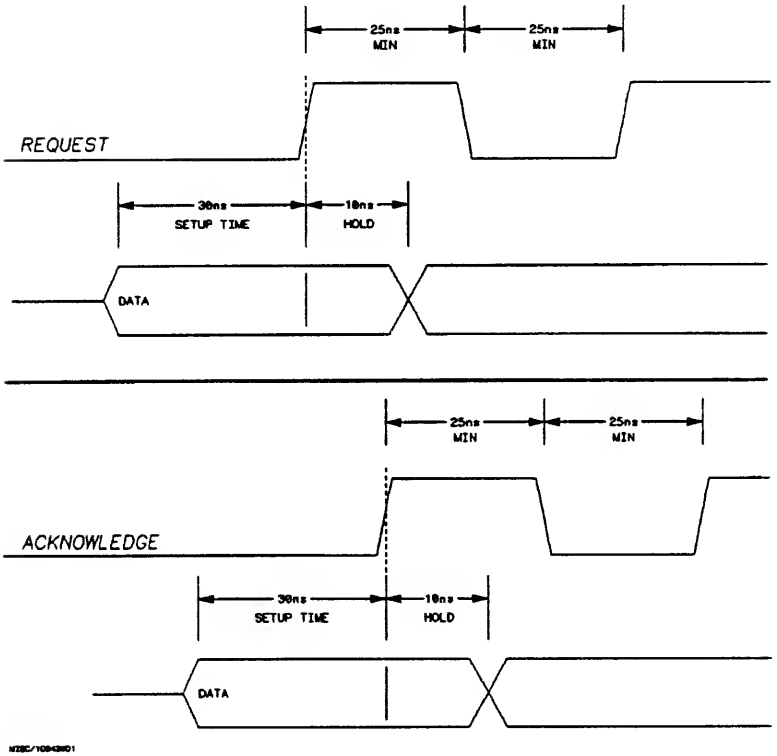


Figure A-4. Request and Acknowledge Timing

Note

The Request and Acknowledge lines in figure A-4 are shown as they would appear on the HP 10343B. These lines are inverted from the actual lines in the SCSI bus.

Reset and Bus Free. When the SCSI Bus is in the Bus Free State and Reset is true, a clock pulse is generated. The D Flip-Flop U18 is put into the reset state when the bus goes free. The reset line is inverted by U10D and is low true ANDed into the OR Gate U7A with the low true Q output of U18. This condition causes a 25 ns pulse at the output of U9C by delaying one of its inputs with the delay line U16 and the inverter U10B. The delay line U8A delays the clock to provide enough setup time for the information-transfer bit into the logic analyzer inputs.

If the SCSI Bus is in the Bus Free State and Reset becomes enabled, all of the lines on the SCSI Bus are latched into the logic analyzer 45 nanoseconds after Reset became active.

Reset is captured by the logic analyzer if it is asserted before an analyzer clock. Otherwise, an extra analyzer clock is generated when the bus goes into the Bus Free phase. The logic analyzer will print "Reset Bus Free" for that state.

All of the lines on the SCSI Bus are latched into the logic analyzer 450 nanoseconds after both Busy and Select become released if Reset is also true at that same time. If Reset is not true, no logic analyzer clock is generated while entering the Bus Free State.

The information-transfer bit (INF) is generated inside of the HP 10343B to differentiate between the Arbitration phase and the Data Out phase on the Status lines. The Busy line is not sent to the logic analyzer state input since it is not required to decode the SCSI phases with the INF bit available.

INF is accomplished with the D Flip-Flop U18. This flip-flop is set when the bus goes into its information phases after the Select or Reselect phase. This always occurs when Select is high in the D input and is stored by Busy going high at the end of the Select or Reselect phase. The logic analyzer does not see this as a info-xfer phase because this happens at the end of the phase and the analyzer is clocked at the beginning of the phase.

The bus is out of the information-transfer (INF) phases when it returns to a Bus Free State. The bus is free when Busy and Select are false for a period of 400nS. U18 is reset at this time through the OR Gates U7B and C, and the 400nS delay line U8B.

All of the conditions that can cause a logic analyzer clock must be output on one line. This is accomplished by ANDing them together with the AND Gates U9A and U9B.

Note

Some states may not capture the ATN signal. In an information output phase where the initiator is sending information, the HP 10343B generates the logic analyzer clock on the asserted edge of Acknowledge. If ATN is true when Request becomes asserted, but ATN goes false before Acknowledge is asserted, ATN may not be captured as true in that state.

Testing and Troubleshooting

There are no established field testing procedures for the HP 10343B. The HP 10343B is part of the Board Exchange Program. This program allows you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. If your instrument is inoperative, contact the nearest Hewlett-Packard Sales and Service Office for assistance.

Replaceable Parts

Since the HP 10343B is part of the Board Exchange Program, the only replaceable parts are the major parts and cabling. These are listed in table A-1. The component level parts shown in table A-1 are for reference purposes only. Figure A-5 shows an exploded view of the HP 10343B.

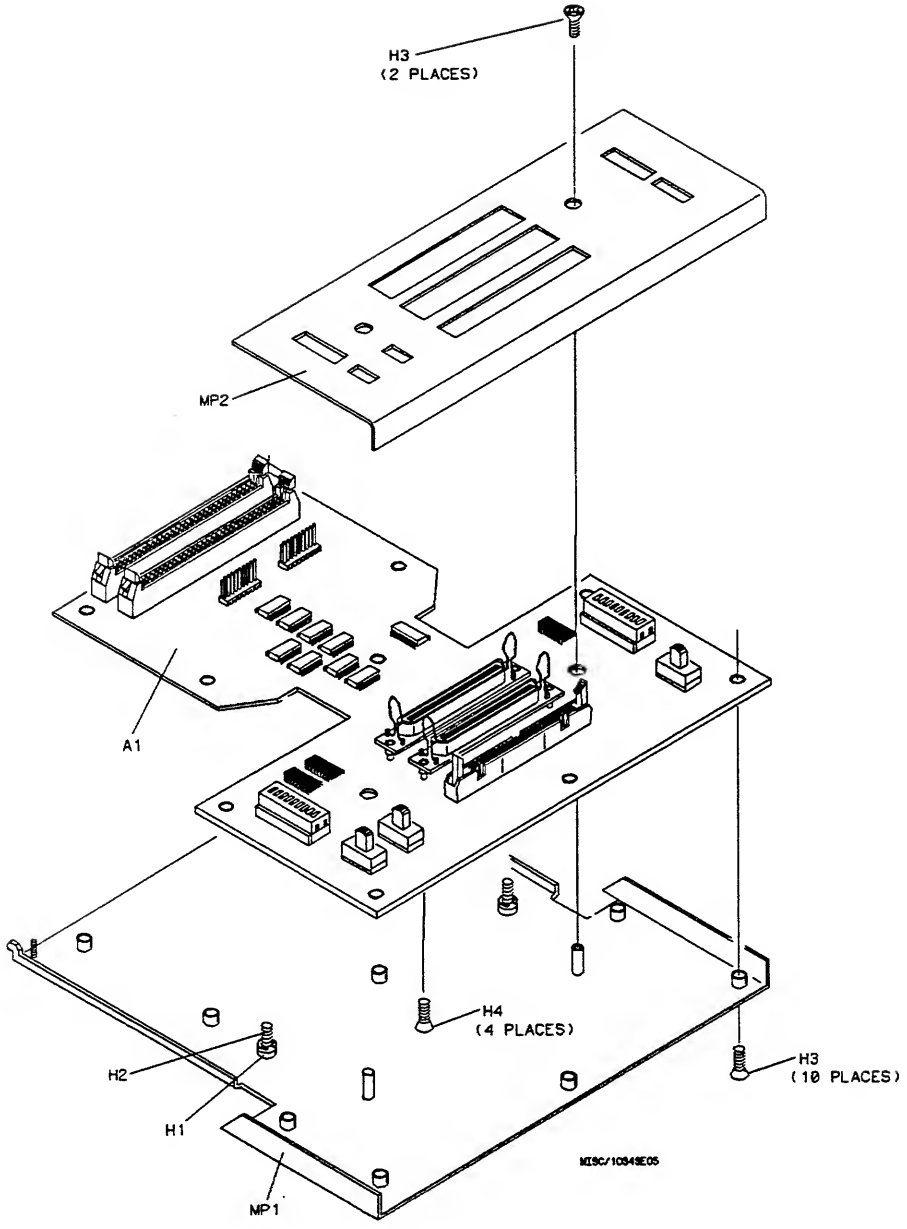


Figure A-5. HP 10343B Exploded View

Table A-1. HP 10343B Parts List

Reference Designator	HP Part Number	Description	Quantity
--	10343-13010	163X Disc Software	1
--	10343-13015	165X Disc Software	1
--	10343-90901	163X Operating Manual	1
--	10343-90902	165X Operating Manual	1
A1	10343-66501	Interface Board Assembly	1
C1	0160-6500	CAP .01 uF 10%	1
C2	0160-6500	CAP .01 uF 10%	1
C3	0160-6500	CAP .01 uF 10%	1
C4	0160-6500	CAP .01 uF 10%	1
C5	0160-6500	CAP .01 uF 10%	1
C6	0160-6500	CAP .01 uF 10%	1
C7	0160-6500	CAP .01 uF 10%	1
C8	0160-6500	CAP .01 uF 10%	1
C9	0160-6500	CAP .01 uF 10%	1
C10	0160-6500	CAP .01 uF 10%	1
C11	0160-6500	CAP .01 uF 10%	1
C12	0180-3848	CF 33 uF	1
C13	0160-6500	CAP .01 uF 10%	1
C14	0160-6500	CAP .01 uF 10%	1
H1	0510-0952	Retainer Ring .094	2
H2	1390-0393	TS Screw Captive	2
H3	2200-0512	Screw 4-40 .312	12
H4	2360-0117	MS 6-32 0.375LG	4
H5	0380-0843	SPACER 4-40 .125	10

Table A-1. HP 10343B Parts List (Continued)

Reference Designator	HP Part Number	Description	Quantity
J1	1252-2076	Conn-Rect 50-CKT 50-CONT	1
J2	1252-2076	Conn-Rect 50-CKT 50-CONT	1
J3	1251-7575	Conn-60 Pin	1
J4	1251-7575	Conn-60 Pin	1
J5	1252-0456	Conn-Post 100-Pin SPR 50-Cont	1
J6	1251-7613	Conn-9 Pin SW	1
J7	1251-7613	Conn-9 Pin SW	1
MP1	10343-04101	Bottom Cover	1
MP2	10343-04102	Top Cover	1
MP3	5951-1125	Label-Serial No.	1
Q1	1854-0215	QN S PL5 2N3904	1
R1	0757-0276	RF .12MF 61.9	1
R2	0698-3442	RF .12CM 237	1
R3	0757-0411	RF .12MF 332	1
R4	0757-0411	RF .12MF 332	1
R5	0757-0453	RF .12MF 30.1K	1
RP1	1810-0272	RES NET 330X9	1
RP2	1810-0272	RES NET 330X9	1
S1	3101-1311	SWSL DPDT	1
S2	3101-1311	SWSL DPDT	1
S3	3101-1313	SWSL DP 3 Throw	1

Table A-1. HP 10343B Parts List (Continued)

Reference Designator	HP Part Number	Description	Quantity
U1	1990-0829	LED-LT Bar	1
U2	1820-1200	IC 74LS05	1
U3	1820-3234	IC 74F280PC	1
U4	1820-2203	IC 26LS32A	1
U5	1820-2203	IC 26LS32A	1
U6	1820-2203	IC 26LS32A	1
U7	1820-2690	IC 74F32	1
U8	1810-1223	400 ns Delay Line	1
U9	1820-2688	IC 74F11	1
U10	1820-1199	IC 74LS04	1
U11	1820-2203	IC 26LS32A	1
U12	1820-2203	IC 26LS32A	1
U13	1820-2203	IC 26LS32A	1
U14	1820-2203	IC 26LS32A	1
U15	1820-2203	IC 26LS32A	1
U16	1810-0828	Delay Line-20 ns MDLDL-TTL-20	1
U17	1820-2684	IC 74F00PC	1
U18	1820-1112	IC 74LS74AN SLT	1
U19	1820-2203	IC 26LS32A	1
U20	1820-2203	IC 26LS32A	1
U21	1820-1200	IC 74LS05	1
U22	1820-1200	IC 74LS05	1
U23	1990-0829	LED-LT Bar	1
U24	1826-0772	IC LM317L	1
UX1	1200-1217	IC Socket-20 Pin	1
UX23	1200-1217	IC Socket-20 Pin	1
W1	8120-4998	Cable Assembly	1

SCSI Overview B

Introduction

The Small Computer Sytems Interface (SCSI) is a standard that may be used for fast transfers of data between Computers and Mass Storage Devices. This includes standards for printers and scanners on the SCSI Bus.

The standard hardware of the 8-Bit SCSI Bus is a 50 wire cable that interconnects up to a maximum of eight devices on the bus. On this cable is defined to be eight data lines with one parity line. Parity is odd and the use of the parity is optional for SCSI.

There are two SCSI Bus Standards:

- Single-Ended; and
- Differential.

The Single-Ended bus runs at TTL levels with a logical 1 (active) being a low level on the bus. The Differential bus uses two lines per signal with the lines moving between approximately 2 and 3 volts.

Each device on the bus is assigned a device number of 1 through 8. If there is a condition of more than one device asking for the bus at one time, the highest numbered device gets the bus. Each device is assigned one line on the data bus for a device ID.

With SCSI, the host computer is not the bus controller. The device that the host calls is the bus controller. Most often this is a mass storage device.

The host computer is called the INITIATOR and the device that the host calls on the bus is called the TARGET.

SCSI Status Lines

Nine status lines are defined by the SCSI Standard X3T9.2/86-109 Revision 2:

- I/O;
- C/D;
- MESSAGE;
- BUSY;
- SELECT;
- REQUEST;
- ACKNOWLEDGE;
- ATTENTION; and
- RESET.

There are also nine phases defined by the SCSI standard. These are not timing phases, but conditions of the bus action. They are:

- ARBITRATION;
- SELECT;
- RESELECT;
- DATA OUT;
- DATA IN;
- COMMAND;
- STATUS;
- MESSAGE OUT; and
- MESSAGE IN.

I/O, C/D, and Message. The I/O, C/D, and Message Status lines define six of these phases of the SCSI Bus (see table B-1).

Busy. The bus is considered free when the Busy and Select lines are inactive. An initiator asks for the bus by driving Busy active and driving its identification (ID) line active on the data lines. If no other device with a higher priority drives the line, then the initiator signals that it has the bus by driving Select active. This is called the Arbitration Phase. The parity bit is not tested in the Arbitration Phase.

Select. After the initiator has the bus and drives Select active it then drives the ID line of the device it is calling (the target) active and releases Busy. The device being called responds by driving Busy active. The Inititor at this point releases Select and Select is not used for anything else. The target device is now in control of the Busy line and is the only device that can release the bus. At this point the bus is ready to transfer information. This is called the Select or Reselect phase. Reselect is when the Target is calling the Initiator. This is accomplished by driving the I/O line active after the Arbitration phase.

Request and Acknowledge. These are handshake lines which are only driven by the target. These handshakes are used to transfer information between devices in either direction. The information that is transferred between devices is enveloped in one of six phases that are determined by the setting of the three lines: I/O, C/D, and Message (see table B-1).

Attention. Since the target is in control of the bus lines, the Attention line (Atn) is used by the Initiator to request to send a Message Out.

Reset. This is used to reset the bus to a Bus Free State and reset the devices that are on the bus.

Note

The SCSI standard includes over 50 commands, 7 Status conditions, and 17 Messages in its instruction set and has room for more to be added. The bus is defined to be capable of transferring 5.5 Megabytes per second.

Table B-1. Phases

Message	I/O	C/D	Name of Phase
0	0	0	Data Out
0	0	1	Data In
0	1	0	Command
0	1	1	Status
1	0	0	Not Defined
1	0	1	Not Defined
1	1	0	Message Out
1	1	1	Message In

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Your Comments Please

HP 10343B

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	Yes	No
1. Did you receive your product when expected?	[ ]	[ ]
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3. Were the proper accessories supplied with your product?

   If not, what was missing?

   Cable(s) [ ] Manual(s) [ ] Other _____

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   _____

5. Which logic analyzer are you using?:

   Type_____

6. What do you like most about the preprocessor?:

   _____

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   [ ] Schematics and Parts List

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   4 = Excellent 3 = Good 2 = Adequate 1 = Poor

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   Please explain:_____

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